3.3 An 118dB DR CT IF-to-Baseband ΣΔ Modulator for AM/FM/IBOC Radio Receivers

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This multi-standard CMOS CT ΣΔ modulator with integrated mixer digitizes a radio signal at a 10.7MHz IF with a DR of 118dB for AM reception, 98dB for FM reception, and a SFDR of 90dB for in-band on-channel (IBOC) reception. The DR of this IF-to-baseband modulator enables the realization of an AM/FM radio without a VGA and without an external AM channel filter, thereby reducing system complexity and cost. Furthermore, the elimination of the VGA improves the radio's NF, increases its sensitivity and reduces its overall power consumption. This modulator combines the anti-aliasing suppression of a CT loop filter with the low jitter sensitivity of a SC-DAC implementation [2].

Figure 3.3.1 (top) shows a state-of-the-art receiver for AM/FM reception [1]. Two radio front-ends mix both AM and FM/IBOC signals to a 10.7MHz IF. The IF signals are filtered by external AM and FM channel filters (30kHz and 200kHz BW) and amplified by a high-linearity/low-noise 0 to 18dB VGA. The same ADC is used in all operating modes with a DR of 100dB for AM and 78dB for FM reception. However, the VGA consumes a few hundred miliwatts and the AM filter is quite costly. To eliminate both, the modulator's DR must be increased by 18dB. This implies that the total in-band noise power of the ΣΔ modulator must be reduced by the same factor. Figure 3.3.1 (bottom) shows the proposed receiver with the 118dB ADC. A VGA is not necessary anymore and a single FM channel filter (200kHz BW) is used, selecting one FM channel or over 20 AM channels.

In order to achieve a noise reduction of 18dB, the input-referred thermal noise impedance of the ADC must be 64 times lower, and so the transconductance (g_m) of the first OTA is scaled proportionally for linearity and noise. The input resistors of the first integrator (an OTA with an RC network) are reduced from few tens of kΩ in [1] to 1.65kΩ. For the same time constant, this requires a significant increase in the size of the integrating capacitors. The passive mixers (Figs. 3.3.2 and 3.3.3) are implemented with NMOS switches placed in between the input resistors and the virtual ground input nodes [3]. High linearity is obtained because the on-resistance of the switches is quite small (16Ω) compared to the input resistances. The lower in-band noise also demands greater immunity to clock jitter. This can be achieved by a SC DAC designed for fast settling [2]. However, the high peak currents (7mA) during the DAC discharge translate to relatively high-amplitude signals across the input virtual ground nodes.

Figure 3.3.2 shows the circuit diagram of the IF-to-baseband system. It consists of two CT ΣΔ modulators and two passive mixers [1], for I/Q demodulation, in a near zero-IF quadrature configuration. The system converts the 10.7MHz IF analog signal into a digital baseband output centred around 275kHz. The 10.425MHz mixing frequency is generated internally from the 41.7MHz sampling frequency. The quantization noise, like the thermal noise, must also be reduced by 18dB. A 5th-order loop filter with both real and complex conjugate poles provides the required quantization noise attenuation within the signal band. The first integrator is implemented with a single-stage telescopic gain-boosted OTA and an RC network for maximum linearity. The other integrators are implemented by G_m-C stages. A 1b quantizer is used together with a 1b inherently linear SC DAC.

Figure 3.3.3 highlights the key circuits connected to the virtual ground input (VGP, VGM) of the IF-to-baseband modulator. To achieve high linearity with the combination of the SC DAC and passive input mixer, the timing of both switched circuits is crucial. The mixer switches are driven by complementary non-overlapping clock phases [3], and change state after the virtual ground nodes have had enough time to settle from the SC DAC discharge. To minimize the effect of double quantization noise sampling, each switch is connected to its own input resistor [1]. The SC DAC is implemented with NMOS-in-n-well floating capacitors and MOS switches. In the first clock phase, the capacitors are charged to $^1/_2$ V_{REF} by closing switches S1 and S3 (switches S2 open). In the second clock phase, switches S2 are closed (switches S1 and S3 open) and the capacitors are discharged in a data-dependent way by closing switches D or DN. To limit the peak currents through the DAC capacitors and to prevent slewing of the first OTA, resistors (R_{DA1}, R_{DA2}) are placed between the capacitors and the data-independent switches S1/S2. A trade-off exists between jitter immunity and the current draw of the first OTA.

The prototype chip (Fig. 3.3.4) is fabricated in a 1P 5M digital 0.18μm CMOS process. The IC includes a clock divider, a DLL, two V_{REF} buffers, and LVDS transmitters. The DLL generates delayed clocks to control the quantizer and the V_{REF} buffers generate 1.6V from an external 1.2V reference. The 41.7MHz clock is provided externally. The modulator operates from a 1.8V supply and consumes 210mW (I+Q). The chip has an active area of 6.0mm^2.

In Fig. 3.3.5, the measured SNDR is plotted as a function of the input signal. In AM mode (3kHz BW) the DR is 118dB and peak SNR is 113dB. In FM mode (200kHz BW) the DR is 98dB and the peak SNR is 90dB. The full-scale (FS) input is $0.5V_{rms}$ (-6dB). Figure 3.3.6 shows the FFT of the measured output bit stream for a two-tone input signal (-6dBFS each tone) with the mixer on (10.675 and 10.725MHz) and the mixer off (250 and 300kHz). With the mixer off (real spectrum), the IM2 is 100dB and the IM3 is 102dB. With the mixer on (complex spectrum), IM2 is 88dB and IM3 is 90dB. For comparison purposes, a CT RTZ DAC is also implemented in this design. In this case the IM2 is 92dB and the IM3 is 94dB (mixer on). The higher noise floor around the down-converted input tones (mixer on) is due to jitter from the signal generator and from the external clock. All the spurious tones inside the signal band are below -100dB. For 20 measured samples, the average image-rejection ratio is 64dB (σ=7dB).

In this paper, a 118dB DR CT IF-to-baseband ΣΔ modulator is described that enables the realization of a highly digitized AM/FM/IBOC radio without a VGA, and without an AM channel filter. Figure 3.3.7 shows the performance summary for this design.

References:

[1] Q. Sandifort, L.J. Breems, C. Dijkmans, H. Schuurmans, "IF-to-Digital Converter for FM/AM/IBOC Radio," *Proc. ESSCIRC*, pp. 707–710, Sept., 2003.

[2] M. Ortmanns, Y. Manoli, F. Gerfers, "A Continuous-Time Sigma-Delta Modulator with Reduced Jitter Sensitivity," *Proc. ESSCIRC*, pp. 287–290, Sept., 2002.

[3] L.J. Breems, E.J. van der Zwan, E.C. Dijkmans, J.H. Huijsing, "A 1.8mW CMOS ΣΔ Modulator with Integrated Mixer for A/D Conversion of IF Signal," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 468–475, Apr., 2000.

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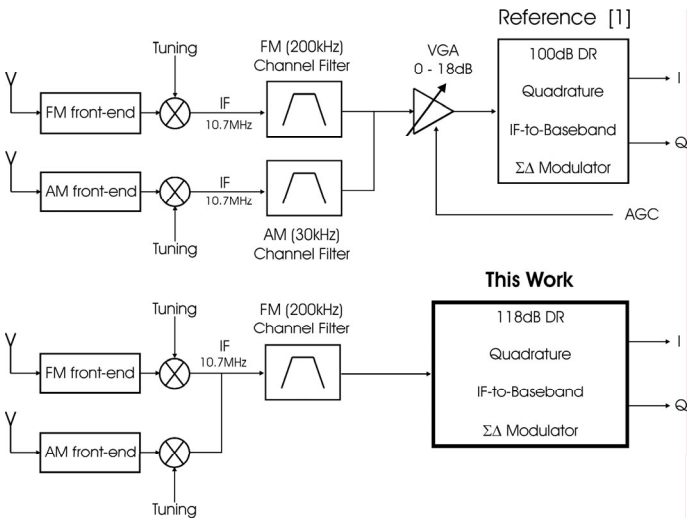

Figure 3.3.1: State-of-the-art AM/FM car radio receiver system (top), new AM/FM car radio receiver system without AGC loop and AM channel filter (bottom).

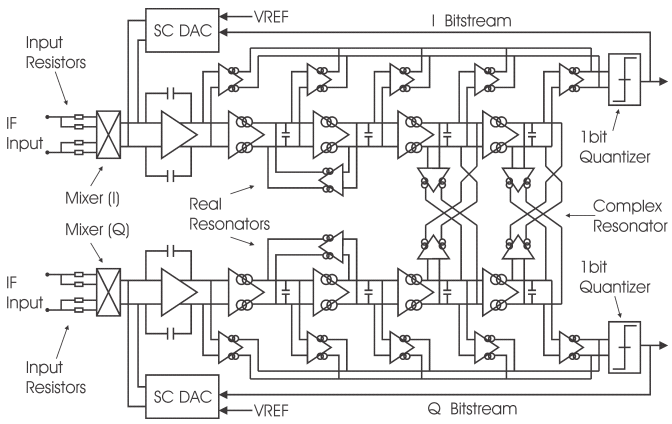

Figure 3.3.2: Quadrature 5th-order 1b CT ΣΔM with SC feedback DAC and integrated IF mixers.

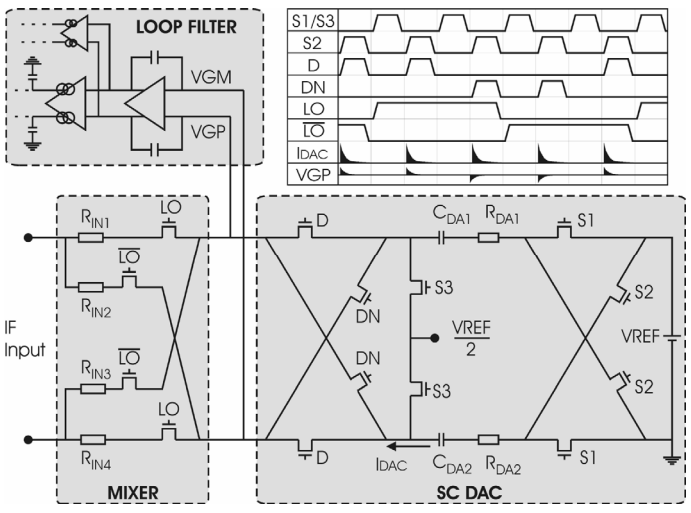

Figure 3.3.3: ΣΔM input stage, IF mixer, SC feedback DAC and timing diagram.

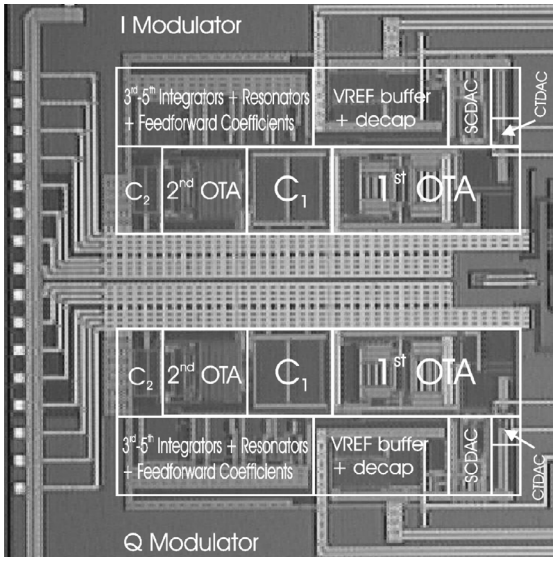

Figure 3.3.4: Die micrograph of the quadrature IF-to-baseband ΣΔM.

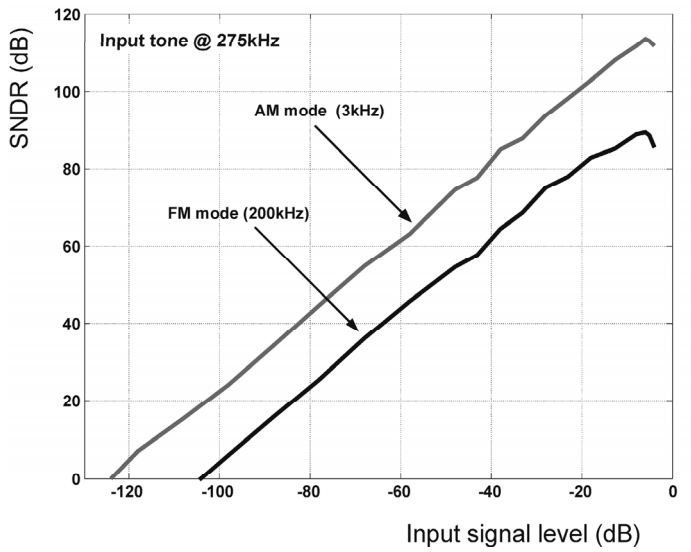

Figure 3.3.5: SNDR as function of input signal level (-6dB = FS).

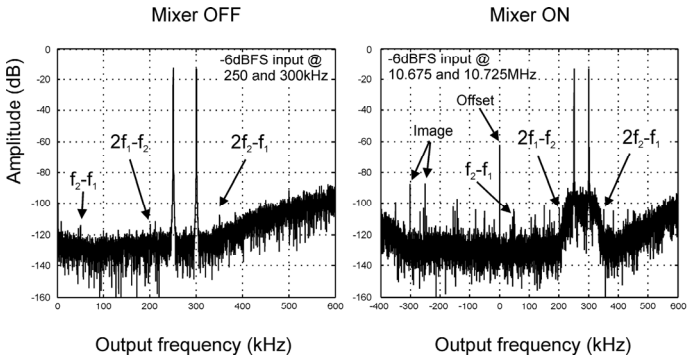

Figure 3.3.6: Intermodulation and image-rejection measurements (RBW = 100Hz).

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Process	1P, 5M, standard 0.18μm CMOS		
Supply Voltage	1.6 - 2.4V		
ΣΔ Modulator	5^{th} order complex CT, 1b with SC DAC		
Input Voltage Range	0.5Vrms, fully differential		
Sampling Rate	41.7MHz		
Mode	**AM**	**FM**	**IBOC**
Signal Bandwidth	3kHz	200kHz	500kHz
DR	118dB	98dB	>70dB
Peak SNDR	113dB	90dB	>70dB
SFDR	>90dB	>90dB	>90dB
Intermod. Distance	**Mixer OFF**	**Mixer ON**	
IM2	100dB	88dB	
IM3	102dB	90dB	
Image Rejection	typical 64dB, σ=7dB		
Active Area	$6.0mm^2$		
Power Consumption	210mW (I+Q)		

Figure 3.3.7: Summary of measured performance.

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